L Number	Hits	Search Text	DB	Time stamp
1	315	(((map$4 near3 technology) and portion) and optimiz$5) and replac$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/13 16:37
2	119	((((map$4 near3 technology) and portion) and optimiz$5) and replac$4) and "716"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/13 16:20
3	0	(((map$4 near3 technology) and portion) and optimiz$5) and 716/$.ccls	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/13 16:38
4	165	(((map$4 near3 technology) and portion) and optimiz$5) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/13 16:38
-	68625	map$4 same (method or technolog$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:54
-	51	(map$4 same (method or technolog$4)) and (divide adj block)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:08
-	3	((map$4 same (method or technolog$4)) and (divide adj block)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:56
-	9975	(map$4 same (method or technolog$4)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:18
-	7730	((map$4 same (method or technolog$4)) and replacement) and block	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:09
-	72	((map$4 same (method or technolog$4)) and replacement) and (sub-network)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:10
-	85	(((map$4 same (method or technolog$4)) and replacement) and block) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:15
-	265	(map$4 same (method or technolog$4)) and (replacement near5 block)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:53
-	7378	map$4 adj3 (method or technolog$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 14:11

-	905	(map$4 adj3 (method or technolog$4)) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:56
-	326	((map$4 adj3 (method or technolog$4)) and replacement) and candidate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:57
-	277	(((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:58
-	275	((((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)) and select$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 10:30
-	3	(((((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)) and select$4) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 10:01
-	19	((map$4 adj3 (method or technolog$4)) and replacement) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 10:01
-	81	(((((map$4 adj3 (method or technolog$4)) and replacement) and candidate) and (block or sub-network)) and select$4) and optimization	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 10:31
-	580	map$4 adj3 technology	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 14:13
-	423	(map$4 adj3 technology) and portion	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 14:14
-	60	(((map$4 adj3 technology) and portion) and optimiz$5) and replacement	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/13 16:18
-	254	((map$4 adj3 technology) and portion) and optimiz$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 14:15

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1	☒	☐	US 20030080990 A1	20030501	28	Navigating heirarchically organized information	345/713
2	☒	☐	US 20030069724 A1	20030410	96	Method and system for debugging an electronic system using instrumentation circuitry and a logic analyzer	703/16
3	☒	☐	US 20030023941 A1	20030130	69	Computer-aided design system to automate scan synthesis at register-transfer level	716/4
4	☒	☐	US 20020178432 A1	20021128	21	Method and system for synthesizing a circuit representation into a new circuit representation having greater unateness	716/18
5	☒	☐	US 20020162086 A1	20021031	19	RTL annotation tool for layout induced netlist changes	716/18
6	☒	☐	US 20020157063 A1	20021024	1889	Implicit mapping of technology independent network to library cells	716/1
7	☒	☐	US 20020156009 A1	20021024	111	Novel interleukin - 1 Hy2 materials and methods	514/12
8	☒	☐	US 20020133788 A1	20020919	29	Structured algorithmic programming language approach to system design	716/3
9	☒	☐	US 6560758 B1	20030506	24	Method for verifying and representing hardware by decomposition and partitioning	716/7
10	☒	☐	US 6546541 B1	20030408	10	Placement-based integrated circuit re-synthesis tool using estimated maximum interconnect capacitances	716/18
11	☐	☐	US 6546539 B1	20030408	13	Netlist resynthesis program using structure co-factoring	716/12
12	☒	☐	US 6543036 B1	20030401	34	Non-linear, gain-based modeling of circuit delay for an electronic design automation system	716/6

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13	☒	☐	US 6539536 B1	20030325	69	Electronic design automation system and methods utilizing groups of multiple cells having loop-back connections for modeling port electrical characteristics	716/18
14	☒	☐	US 6530073 B2	20030304	18	RTL annotation tool for layout induced netlist changes	716/18
15	☒	☐	US 6529861 B1	20030304	24	Power consumption reduction for domino circuits	703/14
16	☒	☐	US 6519609 B1	20030211	12	Method and system for matching boolean signatures	707/104.1
17	☒	☐	US 6505339 B1	20030107	35	Behavioral synthesis links to logic synthesis	716/18
18	☒	☐	US 6496972 B1	20021217	56	Method and system for circuit design top level and block optimization	716/18
19	☒	☐	US 6496842 B1	20021217	25	Navigating heirarchically organized information	715/514
20	☐	☐	US 6490717 B1	20021203	32	Generation of sub-netlists for use in incremental compilation	716/18
21	☒	☐	US 6484292 B1	20021119	10	Incremental logic synthesis system for revisions of logic circuit designs	716/2
22	☒	☐	US 6470482 B1	20021022	42	METHOD AND SYSTEM FOR CREATING, DERIVING AND VALIDATING STRUCTURAL DESCRIPTION OF ELECTRONIC SYSTEM FROM HIGHER LEVEL, BEHAVIOR-ORIENTED DESCRIPTION, INCLUDING INTERACTIVE SCHEMATIC DESIGN AND SIMULATION	716/6

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23	☒	☐	US 6467068 B1	20021015	48	Construction of a technology library for use in an electronic design automation system that converts the technology library into non-linear, gain-based models for estimating circuit delay	716/6
24	☐	☐	US 6446240 B1	20020903	46	Evaluation of a technology library for use in an electronic design automation system that converts the technology library into non-linear, gain-based models for estimating circuit delay	716/2
25	☒	☐	US 6421818 B1	20020716	80	Efficient top-down characterization method	716/18
26	☒	☐	US 6421808 B1	20020716	50	Hardware design language for the design of integrated circuits	716/1
27	☒	☐	US 6389558 B1	20020514	20	Embedded logic analyzer for a programmable logic device	714/39
28	☒	☐	US 6378123 B1	20020423	81	Method of handling macro components in circuit design synthesis	716/18
29	☒	☐	US 6336208 B1	20020101	18	Delay optimized mapping for programmable gate arrays with multiple sized lookup tables	716/16
30	☒	☐	US 6324679 B1	20011127	34	Register transfer level power optimization with emphasis on glitch analysis and reduction	716/18
31	☒	☐	US 6324678 B1	20011127	45	Method and system for creating and validating low level description of electronic design	716/18
32	☒	☐	US 6321369 B1	20011120	24	Interface for compiling project variations in electronic design environments	716/11

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33	☒	☐	US 6321158 B1	20011120	92	Integrated routing/mapping information	701/201
34	☒	☐	US 6311317 B1	20011030	26	Pre-synthesis test point insertion	716/18
35	☒	☐	US 6301687 B1	20011009	27	Method for verification of combinational circuits using a filtering oriented approach	716/3
36	☒	☐	US 6298319 B1	20011002	36	Incremental compilation of electronic design for work group	703/26
37	☒	☐	US 6295636 B1	20010925	82	RTL analysis for improved logic synthesis	716/18
38	☒	☐	US 6295628 B1	20010925	22	Logic synthesis method and device using similar circuit extraction	716/2
39	☒	☐	US 6292931 B1	20010918	81	RTL analysis tool	716/18
40	☒	☐	US 6289498 B1	20010911	81	VDHL/Verilog expertise and gate synthesis automation system	716/18
41	☒	☐	US 6289491 B1	20010911	80	Netlist analysis tool by degree of conformity	716/5
42	☒	☐	US 6263483 B1	20010717	81	Method of accessing the generic netlist created by synopsys design compilier	716/18
43	☒	☐	US 6237127 B1	20010522	40	Static timing analysis of digital electronic circuits using non-default constraints known as exceptions	716/6
44	☒	☐	US 6216252 B1	20010410	53	Method and system for creating, validating, and scaling structural description of electronic device	716/1

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45	☒	☐	US 6205572 B1	20010320	79	Buffering tree analysis in mapped design	716/5
46	☒	☐	US 6182247 B1	20010130	23	Embedded logic analyzer for a programmable logic device	714/39
47	☒	☐	US 6173435 B1	20010109	80	Internal clock handling in synthesis script	716/18
48	☒	☐	US 6166180 A	20001226	22	Chromosome 21 gene marker, compositions and methods using same	530/350
49	☐	☐	US 6134705 A	20001017	32	Generation of sub-netlists for use in incremental compilation	716/18
50	☒	☐	US 6102964 A	20000815	24	Fitting for incremental compilation of electronic designs	716/18
51	☒	☐	US 6086626 A	20000711	30	Method for verification of combinational circuits using a filtering oriented approach	716/5
52	☒	☐	US 6080204 A	20000627	30	Method and apparatus for contemporaneously compiling an electronic circuit design by contemporaneously bipartitioning the electronic circuit design using parallel processing	716/7
53	☒	☐	US 6080201 A	20000627	15	Integrated placement and synthesis for timing closure of microprocessors	703/14
54	☒	☐	US 5983277 A	19991109	33	Work group computing for electronic design automation	709/232
55	☒	☐	US 5933356 A	19990803	43	Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models	703/15
56	☒	☐	US 5917728 A	19990629	28	Method for designing path transistor logic circuit	716/18
57	☒	☐	US 5910898 A	19990608	42	Circuit design methods and tools	716/1

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58	☒	☐	US 5910897 A	19990608	32	Specification and design of complex digital systems	716/19
59	☒	☐	US 5903466 A	19990511	37	Constraint driven insertion of scan logic for implementing design for test within an integrated circuit design	716/18
60	☒	☐	US 5880971 A	19990309	26	Methodology for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from semantic specifications and descriptions thereof	716/6
61	☒	☐	US 5870308 A	19990209	49	Method and system for creating and validating low-level description of electronic design	716/18
62	☒	☐	US 5867399 A	19990202	64	System and method for creating and validating structural description of electronic system from higher-level and behavior-oriented description	716/18
63	☒	☐	US 5838954 A	19981117	85	Computer-implemented method of optimizing a time multiplexed programmable logic device	716/16
64	☒	☐	US 5831868 A	19981103	35	Test ready compiler for design for test synthesis	716/18
65	☒	☐	US 5825662 A	19981020	85	Computer-implemented method of optimizing a time multiplexed programmable logic device	716/3

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66	☒	☐	US 5801958 A	19980901	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/18
67	☒	☐	US 5801957 A	19980901	11	Implicit tree-mapping technique	716/18
68	☒	☐	US 5787010 A	19980728	30	Enhanced dynamic programming method for technology mapping of combinational logic circuits	716/7
69	☒	☐	US 5773268 A	19980630	22	Chromosome 21 gene marker, compositions and methods using same	435/6
70	☒	☐	US 5761484 A	19980602	17	Virtual interconnections for reconfigurable logic systems	716/16
71	☒	☐	US 5761483 A	19980602	85	Optimizing and operating a time multiplexed programmable logic device	716/2
72	☒	☐	US 5734917 A	19980331	17	System for producing combination circuit to satisfy prescribed delay time by deleting selected path gate and allowing to perform the permissible function for initial circuit	716/6
73	☒	☐	US 5729468 A	19980317	35	Reducing propagation delays in a programmable device	716/6

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74	☒	☐	US 5723596 A	19980303	11	European corn borer resistance genetic markers	536/24.3
75	☒	☐	US 5703789 A	19971230	36	Test ready compiler for design for test synthesis	716/4
76	☒	☐	US 5701441 A	19971223	85	Computer-implemented method of optimizing a design in a time multiplexed programmable logic device	716/16
77	☒	☐	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan and near full scan within design for test applications	714/726
78	☒	☐	US 5673200 A	19970930	17	Logic synthesis method and logic synthesis apparatus	716/18
79	☒	☐	US 5648911 A	19970715	10	Method of minimizing area for fanout chains in high-speed networks	716/18
80	☒	☐	US 5630425 A	19970520	50	Systems and methods for adaptive filtering artifacts from composite signals	600/508
81	☒	☐	US 5625567 A	19970429	28	Electronic circuit design system and method with programmable addition and manipulation of logic elements surrounding terminals	716/3
82	☒	☐	US 5623418 A	19970422	66	System and method for creating and validating structural description of electronic system	716/1
83	☒	☐	US 5610829 A	19970311	26	Method for programming an FPLD using a library-based technology mapping algorithm	716/16
84	☒	☐	US 5601088 A	19970211	52	Systems and methods for filtering artifacts from composite signals	600/510

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85	☒	☐	US 5598344 A	19970128	51	Method and system for creating, validating, and scaling structural description of electronic device	716/18
86	☒	☐	US 5596742 A	19970121	15	Virtual interconnections for reconfigurable logic systems	716/16
87	☒	☐	US 5594657 A	19970114		System for synthesizing field programmable gate array implementations from high level circuit descriptions	716/16
88	☒	☐	US 5588152 A	19961224		Advanced parallel processor including advanced support hardware	712/16
89	☒	☐	US 5572437 A	19961105		Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models	716/18
90	☒	☐	US 5572436 A	19961105		Method and system for creating and validating low level description of electronic design	716/18
91	☒	☐	US 5557531 A	19960917		Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation	716/1
92	☒	☐	US 5555201 A	19960910		Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/1

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93	☒	☐	US 5553002 A	19960903		Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface	716/11
94	☒	☐	US 5544067 A	19960806		Method and system for creating, deriving and validating structural description of electronic system from higher level, behavior-oriented description, including interactive schematic design and simulation	703/14
95	☒	☐	US 5544066 A	19960806		Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of low-level design constraints	716/18
96	☒	☐	US 5541850 A	19960730		Method and apparatus for forming an integrated circuit including a memory structure	716/18
97	☒	☐	US 5541849 A	19960730		Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters	716/18
98	☒	☐	US 5537341 A	19960716		Complementary architecture for field-programmable gate arrays	716/16
99	☒	☐	US 5537330 A	19960716		Method for mapping in logic synthesis by logic classification	716/18

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100	☒	☐	US 5526277 A	19960611		ECAD system for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from high-level semantic descriptions thereof	716/3
101	☐	☐	US 5526276 A	19960611	28	Select set-based technology mapping method and apparatus	716/17
102	☒	☐	US 5521835 A	19960528	32	Method for programming an FPLD using a library-based technology mapping algorithm	716/17
103	☒	☐	US 5513124 A	19960430	37	Logic placement using positionally asymmetrical partitioning method	716/7
104	☒	☐	US 5502648 A	19960326	38	Data processing method of generating integrated circuits using prime implicants	716/17
105	☒	☐	US 5498979 A	19960312	15	Adaptive programming method for antifuse technology	326/38
106	☒	☐	US 5493508 A	19960220	31	Specification and design of complex digital systems	716/5
107	☒	☐	US 5490268 A	19960206	17	Method for changing an arrangement of an initial combinational circuit to satisfy prescribed delay time by computing permissible functions of output gates and remaining gates	713/401
108	☒	☐	US 5471398 A	19951128	14	MTOL software tool for converting an RTL behavioral model into layout information comprising bounding boxes and an associated interconnect netlist	716/21

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109	☒	☐	US 5465204 A	19951107	11	Heuristic control system employing expert system, neural network and training pattern generating and controlling system	700/32
110	☒	☐	US 5461577 A	19951024	34	Comprehensive logic circuit layout system	716/17
111	☒	☐	US 5457638 A	19951010	7	Timing analysis of VLSI circuits	716/6
112	☒	☐	US 5452239 A	19950919	131	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementation of the netlist in a hardware emulation system	703/19
113	☒	☐	US 5396435 A	19950307	12	Automated circuit design system and method for reducing critical path delay times	716/6
114	☒	☐	US 5349248 A	19940920	14	Adaptive programming method for antifuse technology	326/38
115	☒	☐	US 5345393 A	19940906	32	Logic circuit generator	716/18
116	☒	☐	US 5224056 A	19930629	33	Logic placement using positionally asymmetrical partitioning algorithm	716/7
117	☒	☐	US 5222030 A	19930622	528	Methodology for deriving executable low-level structural descriptions and valid physical implementations of circuits and systems from high-level semantic specifications and descriptions thereof	716/11
118	☒	☐	US 4803636 A	19890207	22	Circuit translator	716/3
119	☒	☐	US 4703435 A	19871027	16	Logic Synthesizer	716/18